RAPID EVOLUTION OF ANALOG CIRCUITS CONFIGURED ON A FIELD PROGRAMMABLE TRANSISTOR ARRAY

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ABSTRACT

The purpose of this paper is to illustrate evolution of analog circuits on a stand-alone board-level evolvable system (SABLES). SABLES is part of an effort to achieve integrated evolvable systems. SABLES provides autonomous, fast (tens to hundreds of seconds), on-chip circuit evolution involving about 100,000 circuit evaluations. Its main components are a JPL Field Programmable Transistor Array (FPTA) chip used as transistor-level reconfigurable hardware, and a TI DSP that implements the evolutionary algorithm controlling the FPTA reconfiguration. The paper details an example of evolution on SABLES and points out to certain transient and memory effects that affect the stability of solutions obtained reusing the same piece of hardware for rapid testing of individuals during evolution.

1. INTRODUCTION

An evolvable hardware system is constituted of two main components: the reconfigurable hardware (RH) and the reconfiguration mechanism (RM). Figure 1 illustrates several ways of implementing the two components. In previously reported research the evolutionary processor (EP) that acts as a RM was implemented on a variety of platforms including supercomputer (Keymeulen, 2000), single PC (most of researchers, see e.g. (Thompson, 1999)), DSP FPGA and ASIC. The RH was approached as simulated model of unconstrained topology, real FPGA, FPAA model or actual chips (Thompson, 1999), FPTA model or actual chip (Stoica, 2001A).

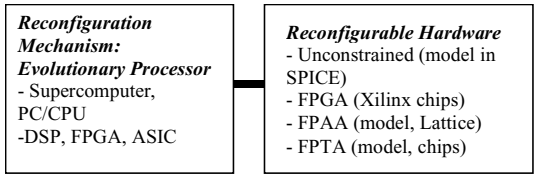

Figure 1. A block diagram of an EHW system

Real-world applications will require compact, low-power, autonomous evolvable hardware. An effort in transitioning from PC -simulated or PC-controlled evolutions to embedded and ultimately to integrated system-on-a-chip evolvable systems is needed.

This paper describes the results of such an integrated effort. The SABLES solution provides autonomous, fast (1,000 circuit evaluations per second), on-chip circuit reconfiguration. Its main components are a JPL Field Programmable Transistor Array (FPTA) chip as transistor-level reconfigurable hardware, and a TI DSP implementing the evolutionary algorithm as the controller for reconfiguration. SABLES achieves approximately 1-2 orders of magnitude reduction in memory and about 4 orders of magnitude improvement in speed compared to systems evolving in simulations, and about 1 order of magnitude reduction in volume and 1 order of magnitude improvement in speed (through improved communication) compared to a PC controlled system using the same FPTA chips.

The paper is organized as follows: Section 2 overviews the components of SABLES, including the FPTA2 chip and the DSP system. The evolution of a half-wave rectifier circuit is presented to illustrate how the system functions. Section 3 concentrates on some stability and reproducibility aspects of solutions evolved by rapid testing of candidate solutions on the same piece of hardware.

2. A STAND-ALONE BOARD LEVEL EVOLVABLE SYSTEM

2.1 SABLES components

SABLES integrates an FPTA and a DSP implementing the Evolutionary Platform (EP) as shown in Figure 2. The system is stand-alone and is connected to the PC only for the purpose of receiving specifications and communicating back the results of evolution for analysis.

Figure 2 Block diagram of a simple stand-alone evolvable system.

The FPTA is an implementation of an evolution-oriented reconfigurable architecture (EORA) (Stoica, 2001A). The lack of evolution-oriented devices, in particular for analog, has been an important stumbling block for researchers attempting evolution in intrinsic mode (with evaluation directly in hardware). Extrinsic evolution (using simulated models) is slow and scales badly when performed accurately e.g. in SPICE), and less accurate models may lead to solutions that behave differently in hardware than in software simulations. The FPTA has transistor level reconfigurability, supports any arrangement of programming bits without danger of damage to the chip (as is the case with some commercial devices). Three generations of FPTA chips have been built and used in evolutionary experiments. The latest chip, FPTA-2, consists of an 8x8 array of reconfigurable cells. Each cell has a transistor array as well as a set of programmable resources, including programmable resistors and static capacitors. Figure 3 provides a broad view of the chip architecture together with a detailed view of the reconfigurable transistor array cell. The reconfigurable circuitry consists of 14 transistors connected through 44 switches and is able to implement different building blocks for analog processing, such as two- and three-stage OpAmps, logarithmic photo detectors, or

Gaussian computational circuits. It includes three capacitors, Cm1, Cm2 and Cc, of 100fF, 100fF and 5pF respectively. Details of the FPTA can be found in Stoica (2001B).

The evolutionary algorithm was implemented in a DSP that directly controlled the FPTA, together forming a board-level evolvable system with fast internal communication ensured by a 32-bit bus operating at 7.5MHz. Over four orders of magnitude speed-up of evolution was obtained on the FPTA chip compared to SPICE simulations on a Pentium processor (this performance figure was obtained for a circuit with approximately 100 transistors; the speed-up advantage increases with the size of the circuit). The evaluation time depends on the tests performed on the circuit. Many of the evaluation tests performed required less than two milliseconds per individual, which for example on a population of 100 individuals running for 200 generations required only 20 seconds. The bottleneck is now related to the complexity of the circuit and its intrinsic response time. SABLES fits in a box 8" x 8" x 3".

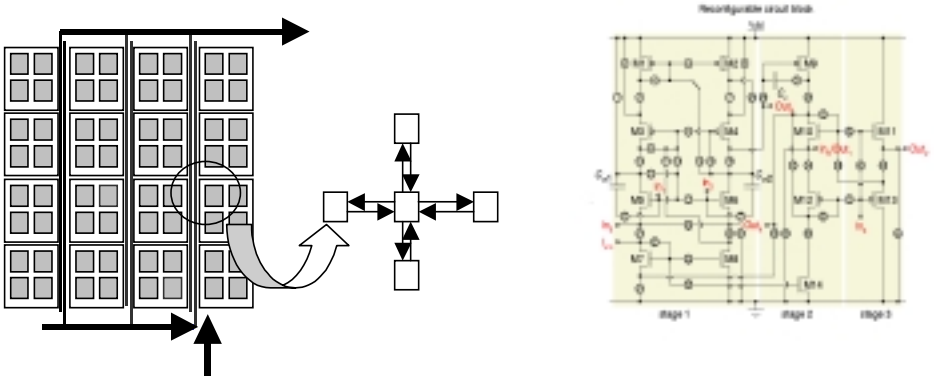

Figure 3. FPTA 2 architecture (left) and schematic of cell transistor array (right). The cell contains additional capacitors and programmable resistors (not shown).

2.2. An Evolution on SABLES

The following experiment illustrates an evolution on SABLES. The objective of this experiment is to synthesize a half-wave rectifier circuit. The testing of candidate circuits is made for an excitation input of 2kHz sine wave of amplitude 2V. A computed rectified waveform of this signal is considered as the target.
The fitness function rewards those individuals exhibiting behavior closer to target (using a simple sum of differences between the response of a circuit and target) and penalizes those farther from it. After evaluation of 100 individuals, they are sorted according to fitness and a 9% portion (elite percentage) is set aside, the remaining individuals undergoing first crossover (70% rate), either among themselves or with an individual from elite, and then mutation (4% rate). In this experiment only two cells of the FPTA were allocated.

The left of Figure 4 depicts the waveforms for stimulus and response, the time allocated for stimulation and the time allocated for the GA in an evolutionary cycle. The right side is the detail, and illustrates the programming time of the new circuit and the stimulation with two periods of waveform, with two different looking responses for the two circuits being evaluated.

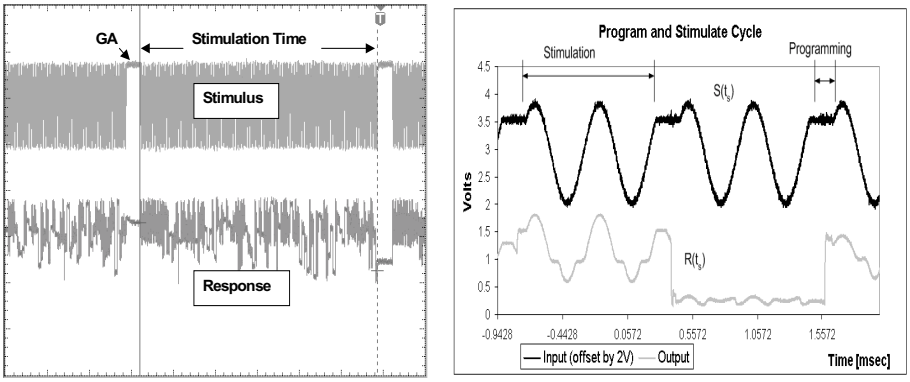

Figure 4 Stimulus-response waveforms during the evaluation of a population in one generation (left) and for 2 individuals in the population (right) A full GA cycle includes stimulus/response (113ms) and the generation of the next generation (6ms). The response was sampled at the maximum sampling rate of the on-board A/D (100kSamp/sec).

Figure 5 displays snapshots of evolution in progress, illustrating the response of the best individual in the population over a set of generations. The first graph shows the best individual of the initial population, while the subsequent ones show the best after 5, 50 and 82 generations. The solution, with a fitness below 4500 (minimum requirement for a satisfactory solution) is shown on the right. Figure 6 shows the convergence over a number of runs.

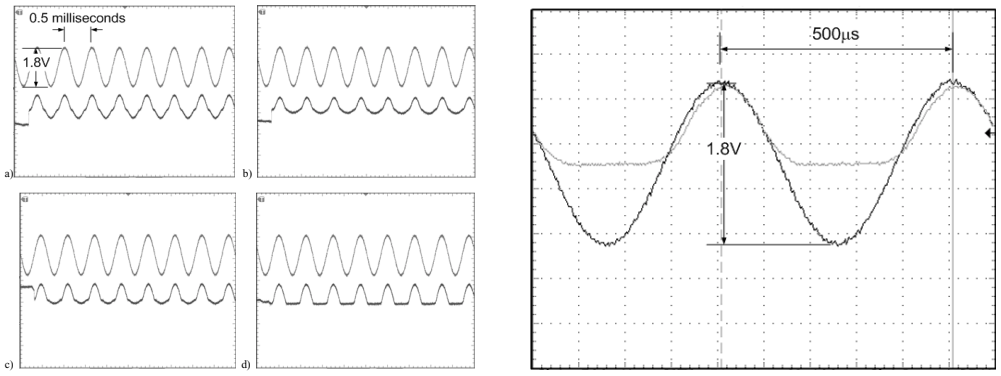

Figure 5 Evolution of a halfwave rectifier showing the response of the best individual of generation a) 1, b) 5, c) 50 and finally the solution at generation d) 82. The final solution is illustrated on the right.

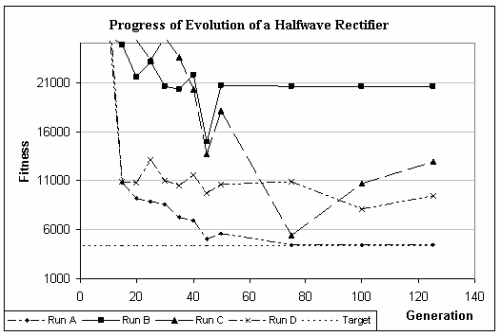

Figure 6 The fitness function as generations progress. The first few generations showed fitness values near 100,000 and are not shown on this scale.

3. ON CERTAIN TRAPS OF EVOLUTIONARY ENGINEERING

The halfwave rectifier experiment provides examples of two situations in which evaluations of candidate solutions on the same hardware-in-the-loop may lead to highly-ranked individuals receiving high fitness function and yet when re-evaluated individually prove to have been only spurious solutions. Figure 7 illustrates both a transient behavior and a FPTA-state dependence. The transient behavior describes a configuration that is not stable as a function of time, whereas FPTA state dependence describes a configuration whose behavior depends on the previous configuration(s). Both of these behaviors are shown in Figure 7; most obviously, the function, which starts out looking similar to a halfwave rectifier ends up looking quite different. The transient behavior in this case occurred on a time-scale of about 1 second. Despite the transient behavior, the individual was selected as a solution because it was evaluated during a time-scale of about 2 milliseconds much shorter than the transient duration. In practice the transient behavior can be resolved by reevaluating the individuals for a longer time period.

The FPTA state dependence behavior occurred when the individual solutions programmed on the FPTA suffer somewhat from an apparent instability, which arises when the evaluation of a given individual depends on the previous state of the FPTA. The individual shown in Figure 7 was selected as a solution because, during the evaluation, its response must have matched quite well the expected function. But part a) of Figure 7 shows that the circuit does not behave sufficiently like the target rectifier, so the behavior exhibited in the evaluation must have been influenced by the previously downloaded configuration(s).

Parasitic as well as static capacitors in the chip explain this behavior. Capacitors can be charged during one configuration period and not discharged before the next configuration is tested, leading to an undefined charge on capacitors and subsequently altering the behavior of the circuit. Nevertheless, for this particular experiment it has been observed that evolution weeds these individuals out and stable solutions are almost always found within the first 50 generations, or about 20 seconds

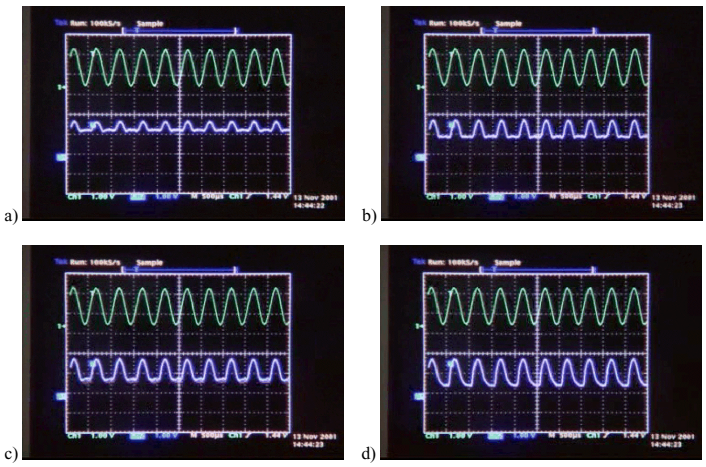

Figure 7 An example of transient behavior. The degradation shown from a) to d) occurred over the span of approximately 1 second.

These results are typical of a series of successful runs. Approximately 1 out of 10 runs ended with the algorithm getting stuck and not finding a solution at all using a fixed mutation rate.

4. SUMMARY AND CONCLUSION

The paper presented a stand-alone board-level evolvable system (SABLES) and illustrated its performance with an evolution time in seconds for a halfwave rectifier circuit. To date this is the fastest, most flexible and most compact stand-alone evolvable system for both analog and digital circuits. Intrinsic evolution using the same hardware-in-the-loop resources for consecutive evaluation of individuals may lead to transient solutions. In most cases these were eliminated simply by allowing extra time for evolution.

Acknowledgements

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